Listing of Claims:

1 – 9 (cancelled)

10. (currently amended) A switching circuit comprising:

at least one switch; and

a controller configured to control a state of said at least one switch with a periodic control signal, ~~said at least one switch responsive to said periodic control signal to change states with a start of each period of said periodic control signal~~, said controller having a skip mode wherein said controller maintains said at least one switch in an OFF state, said controller responsive to a timer, said timer configured to count for a predetermined time interval upon a start of a first period of said periodic control signal, said controller responsive to expiration of said predetermined time interval to disable said skip mode so that said at least one switch changes states at a frequency rate ~~said controller starting a second period of said periodic control signal in response to expiration of said predetermined time interval if said periodic signal has not changed states from said first period, wherein said predetermined time interval is set to achieve a predetermined minimum frequency level of said periodic control signal~~ greater than an audible frequency limit for humans.

11. (original) The circuit of claim 10, wherein said periodic signal comprises a pulse width modulated signal.

12. (currently amended) The circuit of claim 10, wherein said predetermined time interval is about 40 microseconds ~~and said predetermined minimum frequency is about 25 kHz.~~

13. (cancelled)

14. (cancelled)

15. (original) The circuit of claim 10, wherein said timer is coupled between an output terminal of said controller for said periodic control signal and an input terminal of said controller for said skip mode.

16. (original) The circuit of claim 10, wherein said timer is an internal component of said controller.

17. (currently amended) A method ~~of maintaining a minimum frequency of state changes for a switch greater than an audible frequency for humans, said method~~ comprising:

starting a time count of a predetermined time interval at a start of a ~~first~~ state change of ~~said~~ a switch of a DC to DC converter ~~to a first state~~;

monitoring ~~a state of said switch~~ if said switch is in a skip mode; and

disabling said skip mode ~~changing said state of said switch~~ in response to an expiration of said predetermined time interval ~~if said switch is still in said first state to maintain a minimum frequency of said state changes for said switch~~ so that said switch changes states at a frequency rate greater than said audible frequency for humans.

18. (currently amended) The method of claim 17, wherein said predetermined time interval is about 40 microseconds ~~and said predetermined minimum frequency is about 25 kHz~~.

19. (cancelled)

20. (cancelled)

21. (original) A DC to DC converter for converting an input voltage to an output voltage, said DC to DC converter comprising:

a controller configured to provide a PWM signal in a first state during a first time interval based on a first signal representative of said input voltage less a second signal representative of said output voltage;

a driver circuit configured to accept at least said PWM signal and provide a switch driving signal;

a pair of switches including a high side switch and a low side switch responsive to said switch driving signal to drive said pair of switches to a switch ON state where said high side switch is ON and said low side switch is OFF when said PWM signal is in said first state;

an inductor coupled to an output of said pair of switches, wherein a current level in said inductor increases in said switch ON state; and

a logic circuit configured to provide a low side enabling signal having an enabling and disabling state, wherein said PWM signal controls said low side switch when said low side enabling signal is in said enabling state, said logic circuit receiving a comparison signal from an over current comparator, said over current comparator configured to provide said comparison signal based on said current level through said inductor compared to a threshold current value, wherein said logic circuit is further configured to provide said low side enabling signal in said enabling state if said current level in said inductor is greater than said threshold current value.

22. (original) The DC to DC converter of claim 21, wherein said logic circuit comprises a NAND gate.

23. (original) A method of sensing an input voltage level of a DC to DC converter utilizing an existing pin coupled to a switching node of the DC to DC converter, said method comprising:

determining a state of a high side switch coupled to an input voltage source and said switching node;

determining a state of a low side switch coupled between ground and said switching node; and

sensing said input voltage when said high side switch is closed and said low side switch is open.

24. (original) The method of claim 23, wherein said determining steps are based on a state of a pulse width modulated signal that controls said high side and low side switch.

25. (original) A controller for a DC to DC converter, said controller comprising:

an input pin terminal coupled to a switching node of a DC to DC converter, said switching node of said DC to DC converter coupled to an input voltage when a high side switch is closed and a low side switch is open; and

an input voltage sensing circuit coupled to said input pin terminal, said input voltage circuit comprising:

a switch state determination circuit configured to sense when said switching node is coupled to said input voltage based on a state of said high side switch and said low side switch and to provide a determination signal in response thereto; and

a voltage sensing circuit configured to sense a voltage level representative of said input voltage in response to said determination signal representative of said switching node coupled to said input voltage.

26. (original) The controller of claim 25, wherein said switch state determination signal provides said determination signal in response to a state of a pulse width modulated signal that controls a state of said high side and low side switches.

27. (original) A dual phase DC to DC controller comprising:

a first phase controller configured to provide a first PWM signal based on a first signal representative of an input voltage to a DC to DC converter less a second signal representative of an output voltage of said DC to DC converter;

a second phase controller configured to provide a second PWM signal based on said first signal representative of said input voltage to said DC to DC converter less said second signal representative of said output voltage of said DC to DC converter; and

a phase selection circuit configured to select among said first phase controller and said second phase controller.

28 – 30 (cancelled)

31. (new) A method comprising:

starting a time count of a predetermined time interval at a start of a state change of a high side switch of a DC to DC converter;

detecting if said high side switch and a low side switch of said DC to DC converter are in a skip mode; and

disabling said skip mode in response to expiration of said predetermined time interval by closing said low side switch so that said high side switch changes states at a frequency rate greater than an audible frequency limit for humans.

32. (new) The method of claim 31, further comprising controlling said high and low side switches with a periodic control signal, and wherein said closing of said low side switch causes discharging of an output capacitor of said DC to DC converter.

33. (new) The method of claim 32, wherein said periodic control signal comprises a pulse width modulated signal, and wherein a new pulse of said pulse width modulated is generated to turn on said high side switch when a voltage level of said output capacitor decreases to a set voltage level.